REMARKS

Claims 1-18, 20-26 and 28-39 are pending in this broadening reissue application. Claims 1-17 are allowed. Claims 18, 25 and 35 have been amended. Claims 19 and 27 have been cancelled. In view of the following, all pending claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, then the Examiner is requested to schedule a teleconference with the Applicants' attorney to further the prosecution of the application.

Rejection of claims 18, 20-26 and 28-39 under 35 U.S.C. § 112

Claim 18

The Examiner questions on page 2 of the Office Action how "the master latch and the slave latch can recognize the predetermined level of the power." However, it should be noted that claim 18 does not include any language of the master latch and the slave latch recognizing a predetermined level of the power.

It should be noted that claim 18 does not introduce any drastically different language than allowed claim 1. For example, claim 18 recites providing power to an integrated circuit (similar to "integrated circuit device" of allowed claim 1); loading (similar to "load" of allowed claim 1) a first data bit (similar to "first data" of allowed claim 1) into a master latch (similar to "master element" of allowed claim 1) before the power attains a predetermined level (similar to "upon a power-up condition" of allowed claim 1), the master latch being disposed on the integrated circuit (similar to "master element of the integrated circuit device" of allowed claim 1); generating a second data bit (similar to "second data" of allowed claim 1) from the first data bit (similar to "generated by the master element" of allowed claim 1); latching the first data bit in the master latch (similar to "latching in the first data to the master element" of allowed claim 1); and loading the second data bit into a slave latch that is disposed on the integrated circuit (similar to "causing a slave element of the integrated circuit device to load in second data" of allowed claim 1).

For example, referring, *e.g.*, to FIGS. 1-6 of the present application, power is provided to an integrated circuit (which includes clock input buffer 10, input buffer 70,

row address driver circuitry 100, word line and block select latch circuitry 130, word line select circuitry 200, and/or local word line driver circuitry 220). A first data bit 15 is loaded (by input buffer 70) into a master latch 95 before the power attains a predetermined level (upon power-up when master latch 95 initially conducts), the master latch being disposed on the integrated circuit. A second data bit (116 or 128) is generated (by row address driver circuitry 100) from the first data bit. The first data bit is latched (by input buffer 70) in the master latch (when master latch 95 is turned off). The second data bit is loaded (by word line and block select latch circuitry 130) into a slave latch 144 that is disposed on the integrated circuit.

Therefore, claim 18 clearly reads on the specification and drawings.

Claims 25 and 35

Claims 25 and 35 read on the specification and drawings for reasons similar to those recited above in support of claim 18.

Claims 20-22

As discussed above, the second data bit (116 or 128) is generated by the row address driver circuitry 100 (FIG. 3).

For example, referring, *e.g.*, to FIGS. 2-3 of the present application, the second data bit 116 is equal to a complement of the first data bit 15 (col. 5, lines 51-53). In addition, the second data bit 128 is equal to the first data bit 15 (col. 5, lines 53-63).

Claim 29

The Examiner questions on page 3 of the Office Action how "storing and loading steps can generate a test signal." However, it should be noted that claim 29 merely recites that the storing and loading steps comprise (or include) generating a test signal. For example, referring, *e.g.*, to FIGS. 1-4 of the present application, a test (clock) signal 12 is generated (which also provides clock signals 38 and 132).

Claims 30-34

Claims 30-34 read on the specification and drawings for reasons similar to those recited above in support of claim 29.

Claims 32 and 36-39

Claims 32 and 36-39 each have correct antecedent basis. For example, claim 32 recites "wherein loading the first data bit into the master latch comprises..." This is the same "loading the first data bit into the master latch" recited in claim 25.

Allowable Subject Matter

Claim 18

Claim 18 has been amended to include the limitations of allowable claim 19. As indicated by the Examiner, claim 18 is now in condition for allowance.

Claim 25

Claim 25 has been amended to include the limitations of allowable claim 27. As indicted by the Examiner, claim 25 is now in condition for allowance.

Claim 35

Claim 35 has been amended to include similar limitations of allowable claim 19. As indicated by the Examiner, claim 35 is now in condition for allowance.

Claims 20-24, 26, 28-34 and 36-39

Claims 20-24, 26, 28-34 and 36-39 are patentable by virtue of their respective dependencies from claims 18, 25 and 35.

CONCLUSION

In light of the foregoing, claims 1-18, 20-26 and 28-39 are in condition for allowance, and that action is respectfully requested.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner contact the Applicants' attorney at (425) 455-5575.

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Respectfully submitted,

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